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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,380	10/30/2001	Hassan Hashemi	01CON288PC	4071

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EXAMINER
TRAN, THANH Y

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 06/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,380	HASHEMI ET AL.	
	Examin r	Art Unit	
	Thanh Y. Tran	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *91-119* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *111-119* is/are allowed.

6)☒ Claim(s) *91-110* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 91-110 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Applicant's specification fails to teach "a second discrete component embedded in said single interconnect substrate" (emphasis added). This wording is found in independent claim 91. A look at figure 1 yields only an understanding that first and second discrete components 106 surface mounted on the single interconnect substrate 102. None of the drawings of the invention show that a second discrete component embedded in said single interconnect substrate.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 91-110 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuoka (U.S. 5,818,699) in view of Sunahara (U.S. 6,153,290).

With respect to claims 91 and 96, Fukuoka teaches an integrated module (Fig. 8) comprising: a single interconnect substrate (101); a first active circuit chip (202a) wire bonded to the single interconnect substrate (101); a first discrete component (202b) surface mounted on the single interconnect substrate.

Fukuoka does not teach a second discrete component embedded in the single interconnect substrate; and wherein second discrete component is selected from the group consisting of an inductor, a transformer, a capacitor, and a resistor. However, Sunahara teaches a single interconnect substrate (Fig. 1) comprising a discrete component (12 or 10 or 11) embedded in the single interconnect substrate (see Fig. 1, col. 5, lines 29-40); and wherein second discrete component (12 or 10 or 11) is selected from the group consisting of an inductor, a capacitor, and a resistor. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the single interconnect substrate of Fukuoka by providing a discrete component which is selected the group consisting of an inductor, a capacitor, and a resistor and is embedded in the single interconnect substrate as taught by Sunahara for the purpose of producing a high-density multi-layer substrate with stable characteristics

With respect to claim 92, Fukuoka teaches an integrated module (Fig. 8) wherein the first discrete component (202b) is surface mounted using a high-temperature solder (108) (see col. 16, lines 20-25).

With respect to claim 93, Fukuoka teaches an integrated module (Fig. 8) further comprising a solder mask area (sealing pattern 109) on the single interconnect substrate (101) (see col. 15, lines 23-27).

With respect to claim 94, figure 8 of Fukuoka shows that the solder mask area (109) is adjacent to the first discrete component (202b).

With respect to claims 95 and 107-108, Fukuoka teaches an integrated module (Fig. 8) wherein at least one of plurality of metal layers defines the first discrete component (202b); and wherein the first discrete component (202b) is selected from the group consisting of a resistor (see col. 16, line 57).

With respect to claim 97, figure 8 of Fukuoka shows that the single interconnect substrate (101) comprises a plurality of metal layers (104) and a plurality of dielectric layers (as labeled) (see col. 16, lines 61-66).

With respect to claims 98-99 and 109-110, Fukuoka does not teach at least one of the plurality of metal layers defines a printed component/discrete component; and the printed component is selected from the group consisting of an inductor, a resistor, a capacitor, and a transformer. However, Sunahara teaches a single interconnect substrate (Fig. 1) comprising a plurality of metal layers (12, 14, 15, 16, 17, 18) defines a printed component/discrete component; and the printed component (12) is selected from the group consisting of a resistor (see col. 5, lines 35-37).

With respect to claim 100, Fukuoka does not teach the at least one of the plurality of metal layers defines a ground plane. The Examiner takes Official Notice that it is known to include a ground plane in a single interconnect substrate. Thus, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the single interconnect substrate of Fukuoka by including a ground plane for the purpose of reducing capacitive reactance contribution between the layers of the single interconnect substrate.

With respect to claims 101, 102, 104 and 105, Fukuoka does not teach the first active circuit chip comprises RF & IF sections; and second active circuit chip comprises RF & IF sections. The Examiner takes Official Notice that it is known to provide a single interconnect substrate with a first active circuit chip comprising RF & IF sections; and second active circuit chip respectively comprises RF & IF sections. Thus, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the device of Fukuoka by including RF and IF sections in first active circuit chip and second active circuit chip for the purpose of providing first and second active circuit chips with different performing functions at different frequencies for higher levels of circuit integration.

With respect to claim 103, Fukuoka teaches an integrated module (Fig. 8) further comprising a second active circuit chip (see col. 17, lines 10-20). It should be noted that: since Fukuoka teaches an integrated module (Fig. 8) comprising a plurality of active circuit chips (202a), thus the module also includes a second circuit chip.

With respect to claim 106, Fukuoka does not teach first active circuit chip comprises a CMOS chip and wherein the second active circuit chip comprises a GaAs chip. The Examiner takes Official it is known to have first active circuit chip comprises a CMOS chip and wherein the second active circuit chip comprises a GaAs chip. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the device of Fukuoka by including a CMOS chip and a GaAs chip for the purpose of intended use.

Allowable Subject Matter

5. Claims 111-119 are allowed.

The following is an examiner's statement of reasons for allowance: In claims 111-119, the patentability is a combination of: An integrated module comprising a single interconnect substrate including a plurality of metal layers and a plurality of dielectric layers; first and second active circuit chips on a top surface of the single interconnect substrate; a conductive ring formed on the single interconnect substrate, the conductive ring enclosing the first and second active circuit chips; a conductive strip formed on the single interconnect substrate, the conductive strip situated between the first and second active circuit chips; a metal lid covering the first and second active circuit chips, the metal lid contacting the conductive ring and the conductive strip, wherein the metal lid, the conductive ring, and the conductive strip substantially prevent electromagnetic interference from reaching the first and second active circuit chips.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (703) 305-4757. The examiner can normally be reached on Monday through Thursday and on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Martin, can be reached on (703) 308-3121. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3431.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TYT

DAVID MARTIN
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